Motorcomm YT8614C/YT8614H Product Brief

Integrated Quad 10/100/1000M Ethernet Combo Transceiver

Overview

The YT8614 integrates quad independent 10/100/1000M Ethernet transceivers and four SerDes interface into a single IC, and performs all the physical layer (PHY) functions for 1000BASE-T, 100BASE-TX, and 10BASE-Te Ethernet on category 5E UTP cable except 1000BASE-T half-duplex. 10BASE-Te functionality can also be achieved on standard category 3 or 4 cable.
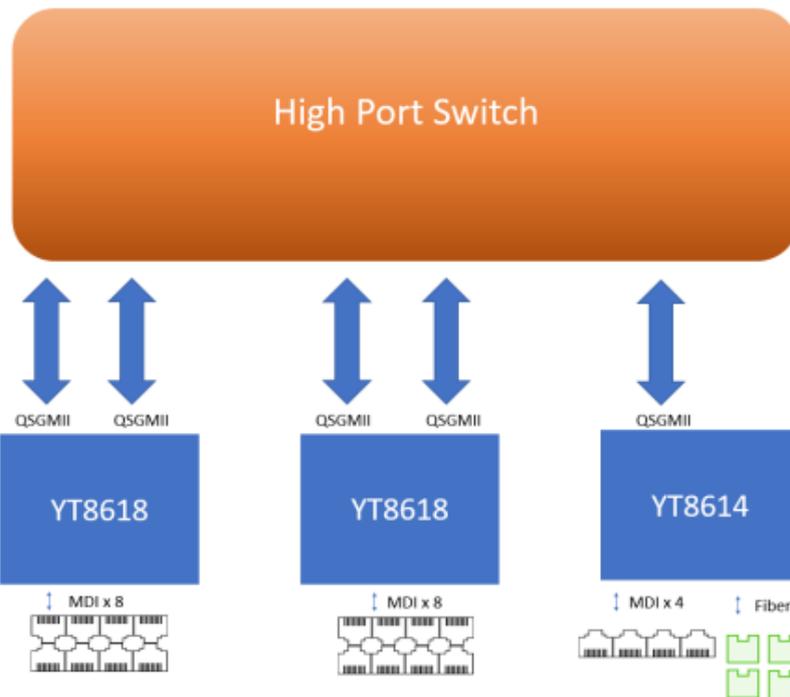
This device also supports four dual media ports and can support up to four 100BASE-FX, 1000BASEX. This device includes PCS, PMA, and PMD sub-layers. They perform encoding/decoding, clock/data recovery, digital adaptive equalization, echo cancellers, crosstalk elimination, and line driver, as well as other required supporting circuit functions. The YT8614 also integrates an internal hybrid that allows the use of inexpensive 1:1 transformer module.

Each of the four independent transceivers features a comprehensive QSGMII for reduced PCB trace. All transceivers can communicate with the MAC simultaneously through the same QSGMII.
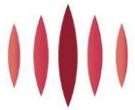
Pin Assignment

Top pins (left to right, 132–89): XTAIU, XTAIO, SGND, SOTXP, SOTXN, SVDDL, SORXP, SORXN, SVDDL, SGND, NC, NC, SGND, NC, NC, SVDDL, SVDDH, SGND, FX3TXP, FX3TXN, SVDDL, FX3RXP, FX3RXN, SGND, FX2TXP, FX2TXN, SVDDL, FX2RXP, FX2RXN, SGND, FX1TXP, FX1TXN, SVDDL, FX1RXP, FX1RXN, SGND, FX0TXP, FX0TXN, SVDDL, FX0RXP, FX0RXN, DVDDL

Left pins (133–176):
- 133 DVDDIO
- 134 RESET_N
- 135 PHYADDR4/LEDCK
- 136 PHYADDR3/LEDDA
- 137 PHYADDR2
- 138 En_PowerOn_Light
- 139 NC
- 140 AVDDH
- 141 P0MDIAP
- 142 P0MDIAN
- 143 P0MDIBP
- 144 P0MDIBN
- 145 AVDDL
- 146 P0MDICP
- 147 P0MDICN
- 148 P0MDIDP
- 149 P0MDIDN
- 150 AVDDH
- 151 P1MDIAP
- 152 P1MDIAN
- 153 P1MDIBP
- 154 P1MDIBN
- 155 AVDDL
- 156 P1MDICP
- 157 P1MDICN
- 158 P1MDIDP
- 159 P1MDIDN
- 160 PLLVDDL0
- 161 NC
- 162 P2MDIAP
- 163 P2MDIAN
- 164 P2MDIBP
- 165 P2MDIBN
- 166 AVDDL
- 167 P2MDICP
- 168 P2MDICN
- 169 P2MDIDP
- 170 P2MDIDN
- 171 AVDDH
- 172 P3MDIAP
- 173 P3MDIAN
- 174 P3MDIBP
- 175 P3MDIBN
- 176 AVDDL

Center: **MOTORCOMM YT8614**

Right pins (88–45):
- 88 DVDDL
- 87 DVDDIO
- 86 CHIP_MODE2
- 85 CHIP_MODE1
- 84 CHIP_MODE0
- 83 MDC
- 82 MDIO
- 81 AVDDH
- 80 NC
- 79 NC
- 78 NC
- 77 NC
- 76 AVDDL
- 75 NC
- 74 NC
- 73 NC
- 72 NC
- 71 AVDDH
- 70 NC
- 69 NC
- 68 NC
- 67 NC
- 66 AVDDL
- 65 NC
- 64 NC
- 63 NC
- 62 NC
- 61 NC
- 60 PLLVDDL1
- 59 NC
- 58 NC
- 57 NC
- 56 NC
- 55 AVDDL
- 54 NC
- 53 NC
- 52 NC
- 51 NC
- 50 AVDDH
- 49 NC
- 48 NC
- 47 NC
- 46 NC
- 45 AVDDL

Bottom pins (1–44, left to right): NC, P3MDICP, P3MDICN, P3MDIDP, P3MDIDN, AVDDH, AVDDH, AGND, RBIAS, AVDDL, SYNCE0, SYNCE1, NC, DVDDIO, DV/DDL, NC, NC, EN_PHY, NC, INTERRUPT, PHYADDR0/SYNC_LOCK0, PHYADDR1/SYNC_LOCK1, NC, DV/DDL, NC, FX3_TX_DIS, FX2_TX_DIS, FX1_TX_DIS, FX0_TX_DIS, NC, DIS_SLED, NC, NC, NC, Reserved, NC, NC, NC, AVDDH, NC, NC, NC, NC, NC

Application Diagram

Key Features

- Integrated Quad 10/100/1000M Ethernet Transceiver with four SerDes interface
- Support QSGMII (Quad Serial Gigabit Media Independent Interface) in 10/100/1000M mode
- Support SGMII mode direct link to one designated Copper Giga PHY with speed adaption
- Physical interface supports 1000BASE-X
- Physical interface supports 100BASE-FX
- Support LRE100-4, disabled by default
  - Cable reach up to 400 meter @100Mbps
- Supports IEEE 802.3az-2010 (Energy Efficient Ethernet)
  - EEE Buffering
  - Incorporates EEE buffering for seamless support of legacy MACs

- Supports crossover detection and auto correction
- Supports auto-detection and auto-correction of wiring pair swaps, pair skew, and pair polarity
- Supports CSD(Cable status diagnostic)
- Supports Link Down Power Saving (Sleep Mode)
- Supports one interrupt output to external CPU for notification
- Supports fast link failure indication
- Supports unidirection in 1000BASE-X/100BASE-FX
- Supports 120m for CAT.5E cable in 1000BASE-T
- Supports Serial LED interface.
- Supports SyncE clock output Mux
  - Recover clock from either SerDes
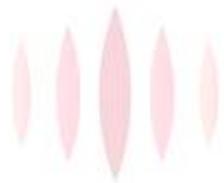 - Recover clock from either Copper PHY

- From internal 25Mhz Clock
- SerDes Test pattern
  - PRBS-7/10/31
  - IDLE /K28.5 /D5.6
  - Customized define by user
  - SerDes BIST
- Packet Generator and Checker

- Low power consumption
- Easy layout, good EMI/EMS, and good thermal performance
- Supports 25MHz crystal or 3.3V OSC input
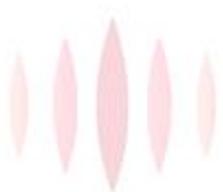- 3.3V and 1.2V power supply
- LQFP-176 E-PAD package

Target Applications

- High Port Density Switch
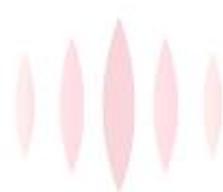- QSGMII MAC
- Copper/Fiber Dual Media